DRAFT

PCI Express® M.2 Specification Revision 4.0 Version 0.5

February 27, 2019

Note to Reviewers:

This specification includes only the high level directions and requirements for the PCI Express 4.0 M.2 specification as approved by the PCIe Mini workgroup. Please provide feedback on these items and any additional requirements that you believe should be covered in the 4.0 M.2 specification.

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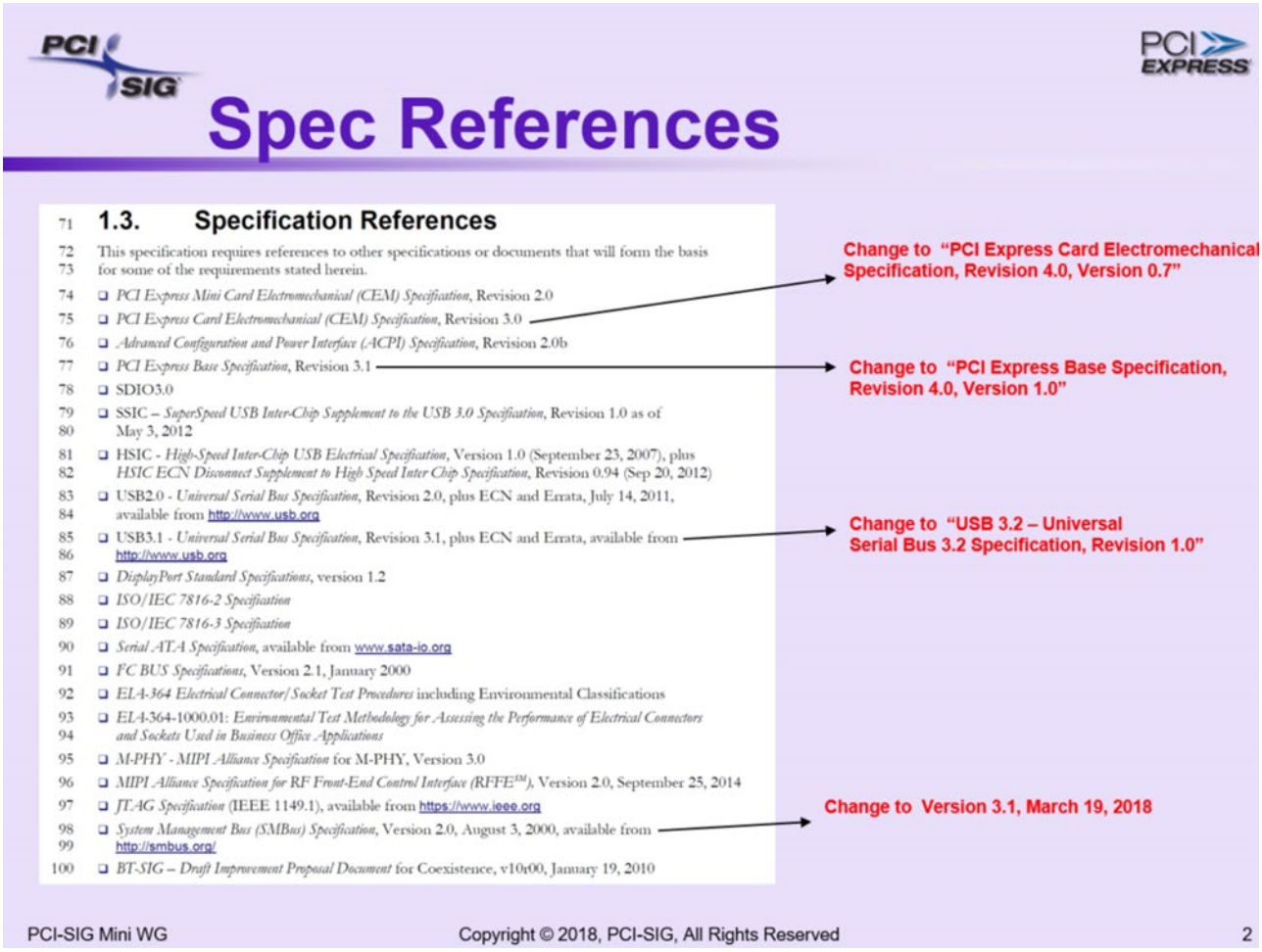
1. **Support signaling rates of 16 GT/s, 8 GT/s, 5 GT/s and 2.5 GT/s**

2. **Specification References list updated to reference the latest specifications:**



3. Clocking

Following clocking architectures will be supported:

a. Common Reference Clock
b. Separate Reference Clock with Independent SSC (SRIS)
c. Separate Reference Clock No SSC (SRNS)

Table 1 shows Clocking Architectures supported by M.2 Platforms and Adapters.

Table 1: M.2 Clocking Architecture Requirements

Clocking Architecture	**PCIe 1.x, 2.x 3.x Adapter**	**PCIe 1.x, 2.x 3.x Platform**	**PCIe 4.0 Platform**	**PCIe 4.0 Adapter**	**Retimer**	**Carrier Card, Riser**
Common Clock	Required	Required	Optional (1)	Required (Default)	Implementation specific	Implementation specific
SRIS	N/A	N/A	Optional (1)	Optional (2)		
SRNS	N/A	N/A	Required if SRIS supported	Optional (2)		

Notes:
1. PCIe 4.0 Platforms must support one or both of these clocking Architectures.

2. PCIe 4.0 Adapters are allowed to support any combination of SRIS and SRNS.

The PCIe 4.0 Adapters are required to support Common Clock as default clocking architecture and are permitted to support SRIS (or SRNS or both). If PCIe 4.0 Adapters support multiple clocking architectures and the reference clock is not detected by the Adapter upon PERST# de-assertion, then PCIe 4.0 Adapters may switch into SRIS (or SRNS) mode.

PCIe 4.0 Platforms are required to support Common Clock architecture or SRIS/SRNS or both (Common Clock and SRIS/SRNS). PCIe 4.0 Platforms supporting SRIS are required to support SRNS. Refer to *PCI Express Base Specification, Revision 4.0.*

If SRIS (or SRNS) is supported by both the PCIe 4.0 Platform and the PCIe 4.0 Adapter, then the PCIe 4.0 Platform is not required to provide the reference clock to the PCIe 4.0 Adapter. The PCIe 4.0 Platform is recommended to terminate the reference clock signals to GND with a pull-down resistor in that case.

Platforms and Adapters that support (PCIe 1.x, 2.x 3.x), are required to support Common Clock architecture only.

Clocking architectures supported for Retimers and Riser/Carrier cards are deemed implementation specific. For retimers, the clocking requirements will be different depending on the location of the retimer. Similarly for Carrier card/Riser implementations, the clocking requirements are determined by end points supported and the primary form factor supported.

Table 2 shows clocking details when supporting Common Clock Architecture. PCIe 1.x, 2.x, 3.x Platforms are required to source clock to the Adapters. PCIe 4.0 platforms, when supporting Common Clock Architecture, are required to source the clock to the Adapters.

Table 2: M.2 Common Clock Architecture Details

Common Clock Details	**PCIe 1.x, 2.x 3.x Platform**	**PCIe 1.x, 2.x 3.x Adapter**	**PCIe 4.0 Platform**	**PCIe 4.0 Adapter**	**Retimer**	**Carrier Card, Riser**
Clock Source	Required	Not Allowed	Required	Not Allowed	Implementation specific	Implementation specific
SSC	Optional	N/A	Optional	N/A		
CLKREQ#	Optional	Optional	Optional	Optional		

CLKREQ# signal is required if L1PM Substates are to be supported. This is applicable for both Common Clock and SRIS/SRNS modes.

4. No connector changes needed to support 16 GT/s on M.2 connectors. Standalone connector Signal Integrity requirements to be updated as follows:

Signal Integrity Parameters and test Procedures for M.2 Connectors

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≥ -0.5 dB up to 4 GHz; ≥ [-0.25*f +0.5 dB for 4 GHz < f < 8 GHz] for example -1.5 dB at 8 GHz ≥ [-0.75*f+4.5 dB for 8 GHz <f<10 GHz For exmple: -3.0 dB at 10 GHz
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≤ -15 dB up to 3.0 GHz; ≤ [5*f - 30 dB for 3.0 < f < 4.4 GHz]. For example: -10 dB at 4 GHz ≤ -8.0 dB from 4.4 to 10 GHz;

NEXT and FEXT at 8GHz

Intra-pair Skew (Soldered-down BGA)	Intra-pair skew must be achieved by design; measurement not required.	1 ps max
Intra-pair Skew (BGA mounted on the M.2 Add-in Card)	Intra-pair skew must be achieved by design; measurement not required.	2 ps max
Differential Near End Crosstalk (DDNEXT) and Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard must be used with the following considerations: • The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. • This is a differential crosstalk between a victim differential signal pair and all adjacent differential signal pairs. The measured differential S-parameter shall be referenced to 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5 GHz; ≤ -20 dB for 5 GHz < f ≤ 10 GHz < -10 dB for 10 GHz < f ≤ 12 GHz

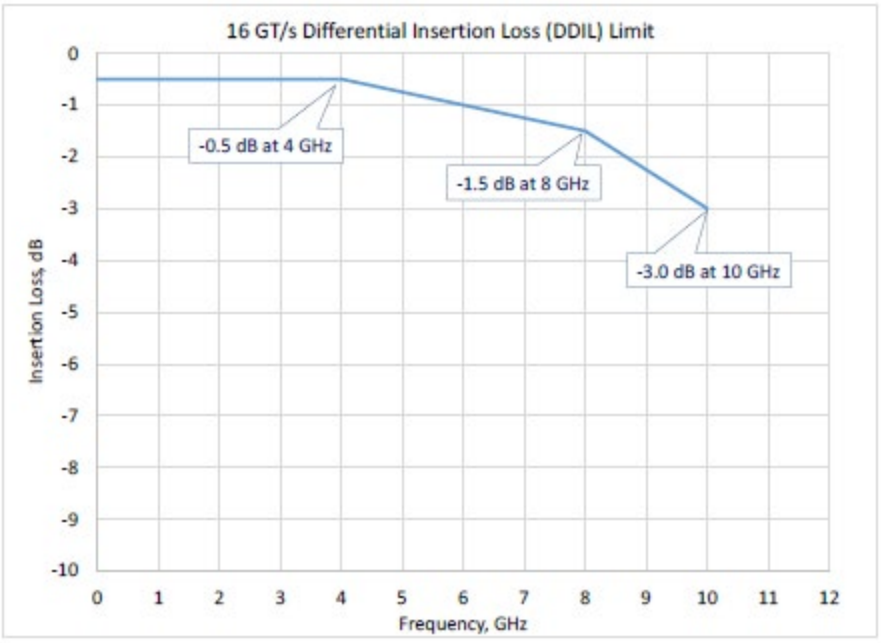


Figure 1: Differential Insertion Loss Limits for 16.0 GT/s Operation

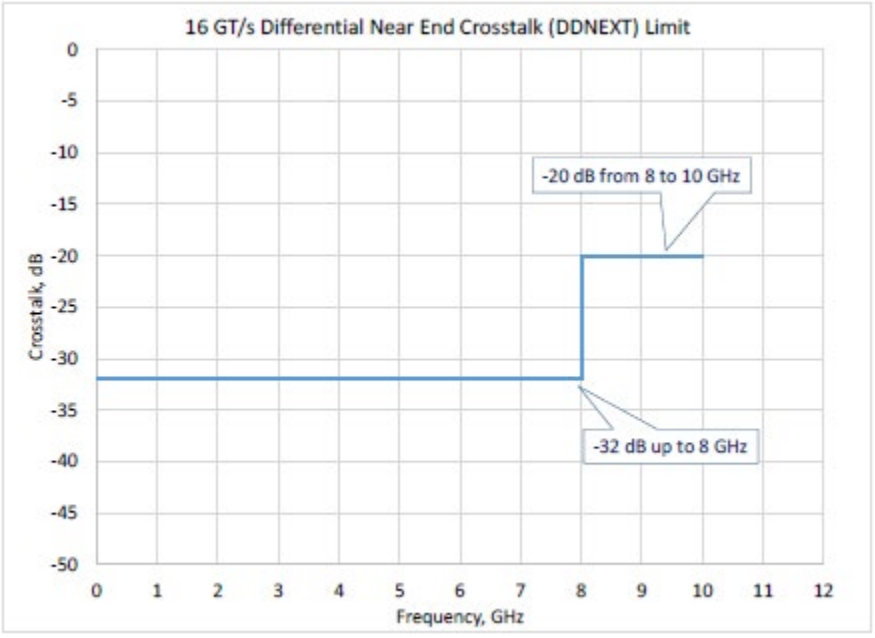


Figure 2: Differential Near End and Far End Crosstalk Limits for 16.0 GT/s Operation

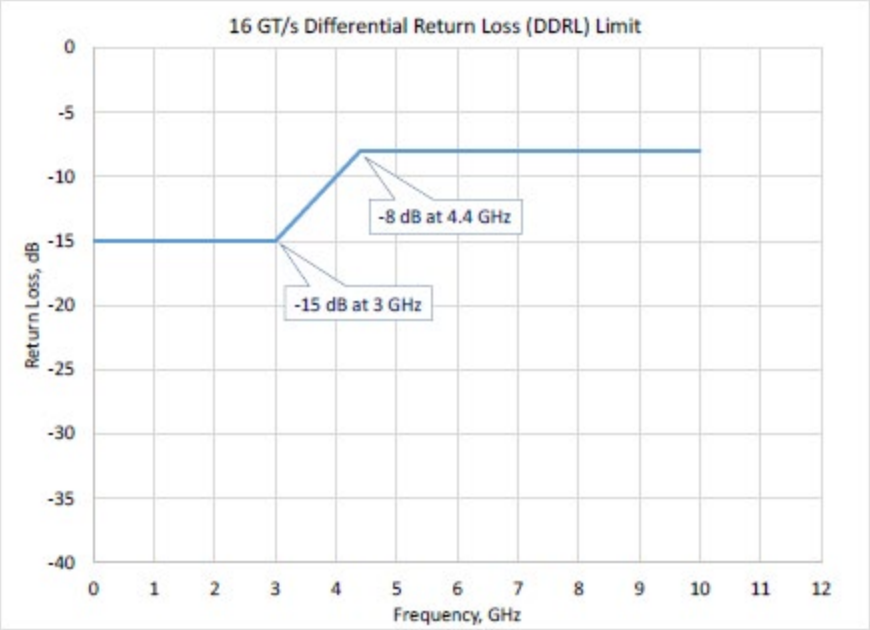


Figure 3: Differential Return Loss Limits for 16.0 GT/s Operation

5. Add following Insertion Loss budget requirements:

5.1 Add-in Card Insertion Loss Limit for 16GT/s

The insertion loss from the top of edge finger to the silicon pad for both Receiver and Transmitter interconnect must not exceed 6.5 dB at 8 GHz for SSDs. Other applications are not required to follow this IL limit but need to make sure that the total IL at 8GHz does not exceed 8dB. This loss includes PCB routing, vias, AC Cap and silicon package.

6. Add Standalone Connector test guidelines in the Signal Integrity section.

Elaborate on the Victim/Aggressor high speed signal pair arrangement to capture worse case cross-talk on the connector. TBD.

7. Update the test fixtures recommendations and golden finger Ground voiding guidelines to support 16 GT/s

TBD.

8. Add Transmitter Equalization details

8.1 Preset Test Requirements at 16.0 GT/s

All Add-in Cards and system boards operating at 16.0 GT/s are required to meet the preset test as described in the *PCI Express Base Specification*. The test consists of acquiring the transmitter compliance waveforms from the device under test for each preset, then analyzing the waveforms together to confirm that the preset requirements have been met.

9. Define Eye Diagrams at the Add-in Card Interface

9.1 Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s

The eye diagrams for the M.2 Add-in Card's Transmitter path compliance at 16.0 GT/s are defined in Table 3. The M.2 Add-in Card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification.* The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification,* are applied.

A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification)* is being transmitted during the test.

Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

The calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.
The values in Table 3 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω FR4 trace with an insertion loss of 16.5 dB at Nyquist., followed by a root reference package all behind a standard M.2 connector. This channel shall be referenced as the 16.0 GT/s M.2 Add-in Card Test Channel. S-parameters for the channel provided with the specification. Additional loss from the measurement set-up must be removed. The M.2 Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a M.2 compliant motherboard.

Table 3: M.2 Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	TBD	1300	mV	Notes 1
V_{TXA_d}	TBD	1300	mV	Notes 1
T_{TXA}	TBD		ps	Notes 2

Notes:
1. The voltage measurements are done at a BER of 10^{-12}.
2. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 2×10^6 UI.

9.2 Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the Add-in Card Receiver path compliance at 16.0 GT/s are defined in Table 4. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.
If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters –then the other parameters must be adjusted back to the calibrated values.
If the test is not run in a way that produces the worst-case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way.

The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run.

Eye height and width are specified after the application of the reference receiver. $V_{RX\text{-}EH\text{-}16G}$ and $T_{RX\text{-}EH\text{-}16G}$ are adjusted following the same process described in the PCI Express Base Specification for calibrating the 16.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 16.0 GT/s stressed eye calibration process the variation must occur in the 16.0 GT/s Add-in Card Test Channel portion of the channel.

The Eye Height and Eye Width values in Table 4 are initially calibrated with a reference channel consisting of an 16.0 GT/s M.2 Add-in Card Test Channel followed by an 16.0 GT/s M.2 System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 16.0 GT/s TX test. After reference calibration, the 16.0 GT/s System-Board Test Channel is removed and the Add-in Card to be tested is placed into a standard PCI Express connector. The end to end M.2 calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 16.0 GT/s calibration channel in the PCI Express Base Specification.

Table 4. Add-in Card Minimum Receiver Path Sensitivity Requirements at 16 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX\text{-}EH\text{-}16G}$ Eye Height	15	15	mV	Notes 1, 2
$T_{RX\text{-}EH\text{-}16G}$ Eye Width	0.3	0.3	UI	Notes 1
Rj (Random Jitter)	1.0		ps RMS	Notes 3, 4
Sj (Sinusoidal Jitter) 100 MHz	6.25		ps PP	Note 4
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	

Notes:
1. An ideal reference clock without jitter is assumed for this specification. Eye height and width values refer to BER of 10^{-12}.
2. Eye height limits do not account for limitations in test equipment voltage resolution.
3. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
4. Rj and Sj are measured without post-processing filters.

9.3 System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the transmitter equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral receiver equalization algorithm defined in the *PCI Express Base Specification* are applied.
The system board Transmitter path measurements at 16.0 GT/s are made using a two-port measurement methodology. Refer to the *PCI Express CEM Specification* for the details of the two-port method.

All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification)* is being transmitted during the test.
Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

The calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.
The values in Table 5 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 3.5 dB of 85 Ω trace, at 8GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 16.0 GT/s System-Board Test Channel. The s-parameters for the channel are provided with this specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

Table 5: System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Unit	Comments
V_{TXS}	TBD	1300	mV	Notes 1
V_{TXS_d}	TBD	1300		Notes 1
T_{TXS}	TBD		ps	Notes 2

Notes:
1. The voltage measurements are done at a BER of 10^{-12}.
2. T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 2 x 10_6 UI.

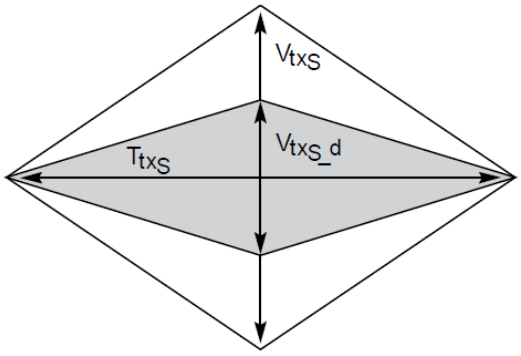


Figure 4: 16.0 GT/s System Board Transmitter Path Composite Compliance Eye Diagram

9.4 System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the system board Receiver path compliance at 16.0 GT/s are defined in Table 6. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using transmitter equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required transmitter equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.
If the test generator's transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters –then the other parameters must be adjusted back to the calibrated values.
If the test is not run in a way that produces the worst-case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way.

The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run.

The Eye Height and Eye Width values in Table 6 are initially calibrated with a reference channel consisting of a 16.0 GT/S M.2 System Board Test Channel followed by a 16.0 GT/s M.2 Add-in Card Test Channel. After reference calibration, the 16.0 GT/s M.2 Add-in Card Test Channel is removed, and the 16.0 GT/s M.2 System Board Test Channel is connected to the system board to be tested. The end to end M.2 calibration channel must meet the requirements (insertion loss

and return loss masks) defined for the 16.0 GT/s calibration channel in the PCI Express Base Specification.

Eye height and width are specified after the application of the reference receiver. $V_{RX-EH-16G}$ and $T_{RX-EH-16G}$ are adjusted following the same process described in the PCI Express Base Specification for calibrating the 16.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 16.0 GT/s stressed eye calibration process the variation must occur in the 16.0 GT/s System Board Test Channel portion of the channel.

Table 6: System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX-EH-16G}$ Eye Height	15	15	mV	Notes 1, 2
$T_{RX-EH-16G}$ Eye Width	0.3	0.3	UI	Notes 1
Rj (Random Jitter)	1.0		ps RMS	Notes 3, 4
Sj (Sinusoidal Jitter) 100 MHz	6.25		ps PP	Note 4
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	

Notes:
1. The system board reference clock is assumed for this specification. Eye height and width values refer to BER of 10^{-12}.
2. Eye height limits do not account for limitations in test equipment voltage resolution.
3. Rj is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.
4. Rj and Sj are measured without post-processing filters.

9.5 Add-in Card Transmitter Path Pulse Width Jitter (PWJ) limits at 16 GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$) at a BER of 10^{-12} are defined in Table 7. The Add-in Card shall pass the timing requirements with the Jitter Measurement Pattern defined in the *PCI Express Base Specification*. The pulse width jitter requirements are evaluated after the -12 dB CTLE curve from the behavioral reference equalizer defined in the *PCI Express Base Specification,* is applied.

Table 7: Add-in Card Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
$T_{TX-UPW-TJ}$	0	12.5	ps PP @ BER 10^{-12}	
$T_{TX-UPW-DJDD}$	0	5.0	ps PP @ BER 10^{-12}	

Additional compliance requirements needed to support SRIS/SRNS will be added in the next version of this specification.

10. Define 16 GT/s Test channels and distribute with the specification.

a. System board test channel with connector (S-parameters)
    i. TBD
b. Add-in Card test channel without connector (S-parameters)
    i. TBD